REMARKS

Claims 1-22 are presently pending in this application.

It is noted that Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

The Examiner objects to the language of claim 15. Although Applicant does not agree with the Examiner, this claim has been amended to expedite prosecution.

Claims 11-14 and 22 are allowed.

Applicant gratefully acknowledges the Examiner's indication that claims 6-9, 18, and 19 would be allowable if rewritten in independent format. However, Applicant believes that all claims are allowed when properly understood and declines to rewrite these claims at this time.

Claims 1, 2, and 21 stand rejected under 35 USC §102(b) as anticipated by US Patent 4,672,647 to Yamaguchi, and claim 10 stands rejected under 35 USC §103(a) as unpatentable over Yamaguchi. Claims 3-5 stand rejected under 35 USC §103(a) as unpatentable over Yamaguchi, further in view of Applicant's Admitted Prior Art (AAPA) and claims 15-17 and 20 stand rejected under 35 USC §103(a) as unpatentable over AAPA, further in view of Yamaguchi.

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor circuit system including a first signal line and n circuit sections, where n is an integer greater than 2, each of which includes an input terminal and an output terminal. The input terminals of only predetermined k ones of the n circuit sections are connected to the first signal line, where k is an integer equal to or greater than 2 and less than n, and the output terminal of an m^{th} one of the n circuit sections is connected to the input terminal of an $(m+k)^{th}$ one of the n circuit sections, where m is an integer varying between 1 and n-k, thereby k of the n circuit sections are activated at a given time.

Conventional horizontal drive circuits activate all n of the circuits, including the time it takes to stabilize the input differential circuits, thereby causing considerable power consumption.

The claimed invention, on the other hand, drives only a predetermined number of the circuits, thereby reducing power consumption with a stable horizontal driving operation.

II. THE PRIOR ART REJECTIONS

The Examiner alleges that Yamaguchi teaches the claimed invention described by claims 1, 2, 21, render obvious claim 10, and, when modified by AAPA, renders obvious claims 3-5. The Examiner also alleges that AAPA, when modified by Yamaguchi, renders obvious claims 15-17 and 20.

Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by Yamaguchi or AAPA.

More specifically, the present invention activates k of the n circuit sections at a given point in time, as can be clearly seen in Figs. 5F and 5G, when k = 2. In contrast, Yamaguchi has phase clocks ϕi so that each element Sij is separately activated, as clearly shown in Fig. 1b.

This feature of the claimed invention allows it to be used in driving columns in a display device, whereas Yamaguchi is not directed toward this environment. The Examiner relies upon AAPA for reasons other than the above identified deficiency.

Hence, turning to the clear language of the claims, in Yamaguchi there is no teaching or suggestion of: " ... thereby k of said n circuit sections are activated at a given time", as required by claim 1. The remaining independent claims have similar language.

Therefore, Applicant submits that there are elements of the claimed invention that are not taught or suggest by Yamaguchi. Therefore, the Examiner is respectfully requested to withdraw this rejection.

Further, Applicant submits that the Examiner can point to no motivation or suggesting in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that "[i]t would have been obvious in order to adapt the shift registers of Yamaguchi to support display driving." Applicant submits that

this motivation is merely improper hindsight, since there is clearly no suggestion in either reference for such combination.

Moreover, relative to the rejection for claim 2, Applicant submits that one having ordinary skill in the art would not agree that the description in Yamaguchi of loading a data value satisfies the plain meaning of the claim language, if for no other reason than that the individual circuit units are not themselves stopping this "operation", since the clock signal controls the data loading. In contrast, as can be seen exemplarily in Figure 6, the present invention has a latch mechanism in each circuit section that serves as an operation timer.

III. FORMAL MATTERS AND CONCLUSION

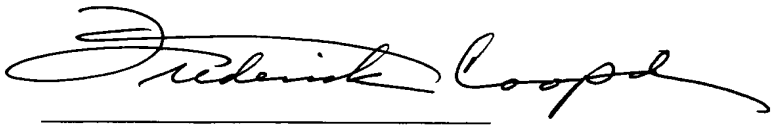
In view of the foregoing, Applicant submits that claims 1-22, all the claims presently pending in the application, are patentably distinct over the prior art of record and that the application is in condition for allowance. Such action would be appreciated.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

To the extent necessary, Applicant petitions for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to Attorney's Deposit Account No. 50-0481 and please credit any excess fees to such deposit account.

Respectfully Submitted,

Date: 5/24/06



Frederick E. Cooperrider
Registration No. 36,769

McGinn Intellectual Property Law Group, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254